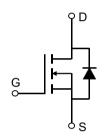
### **Features**

• 120V, 90A

 $R_{DS(ON)}$  Typ = 6.5m $\Omega$  @  $V_{GS}$  = 10V

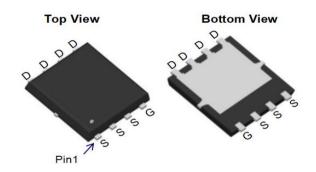
- Advanced Split Gate Trench Technology
- Excellent R<sub>DS(ON)</sub> and Low Gate Charge
- Lead Free
- 100% UIS TESTED!
- 100% ΔVds TESTED!



**Schematic Diagram** 

## **Application**

- Load Switch
- PWM Application
- Power Management



**PDFN5**\*6-8L

#### **Package Marking and Ordering Information**

Device	Marking	Package		Reel Size	Reel (pcs)	Per Carton (pcs)
NS120H06F	NS120H06F	PDFN5x6-8L	TAPING	13"	5000	50000

#### **Absolute Maximum Ratings** (@ T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter		Value	Units
$V_{DS}$	Drain-to-Source Voltage		120	V
$V_{GS}$	Gate-to-Source Voltage		±20	V
	Continuous Dunin Current	T <sub>C</sub> = 25°C	90	А
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 100°C	54	А
I <sub>DM</sub>	Pulsed Drain Current (1)		360	А
E <sub>AS</sub>	Single Pulsed Avalanche Energy (2)		225	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	129	W
$R_{ heta JC}$	Thermal Resistance, Junction to Case		0.97	°C/W
$T_{J}$ , $T_{STG}$	Junction & Storage Temperature Range		-55 to 150	°C

### **Electrical Characteristics** (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Chara	acteristics					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	120	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V	-	-	1.0	μА
I <sub>GSS</sub>	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	±100	nA
On Chara	acteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.4	3	3.6	V
R <sub>DS(ON)</sub>	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 10V, I_D = 30A$	-	6.5	8.5	mΩ
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance		-	2712	-	pF
$C_{oss}$	Output Capacitance	$V_{GS} = 0V, V_{DS} = 60V,$ f = 1MHz	-	815	-	pF
$C_{rss}$	Reverse Transfer Capacitance	1 – 11VII 12	-	7	-	pF
$Q_g$	Total Gate Charge		-	33	-	nC
$Q_{gs}$	Gate Source Charge	$V_{GS} = 0 \text{ to } 10V$ $V_{DS} = 60V, I_{D} = 20A$	-	7	-	nC
$Q_gd$	Gate Drain("Miller") Charge	VDS - 00 V, ID - 2071	-	8	-	nC
Switchin	g Characteristics					
t <sub>d(on)</sub>	Turn-On DelayTime		-	11	-	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10V, V_{DD} = 60V$	-	20	-	ns
$t_{\text{d(off)}}$	Turn-Off DelayTime	$I_D$ = 20A, $R_{GEN}$ = $6\Omega$	-	32	-	ns
$t_f$	Turn-Off Fall Time		-	28	-	ns
Drain-So	urce Diode Characteristics and M	lax Ratings				
Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	90	А
I <sub>SM</sub>	aximum Pulsed Drain to Source Diode Forward Current		-	-	360	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{S} = 30A$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	1 = 15A dild+ = 100A/··-	-	54	-	ns
Qrr	Body Diode Reverse Recovery Charge	$I_F = 15A$ , di/dt = 100A/us	-	58	_	nC

Notes:

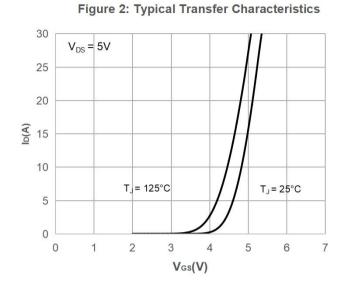
<sup>1.</sup> Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

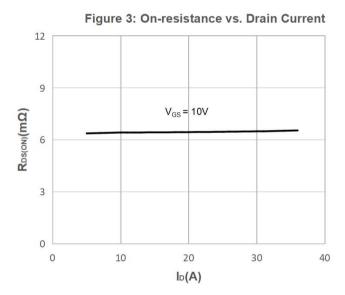
<sup>2.</sup>  $E_{AS}$  condition: Starting  $T_J$ =25°C,  $V_{DD}$ =60V,  $V_G$ =10V,  $R_G$ =25ohm, L=0.5mH,  $I_{AS}$ =30A

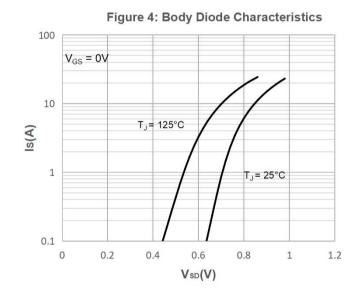
<sup>3.</sup> Pulse Test: Pulse Width  $\!\!\leqslant\! 300\mu s,$  Duty Cycle  $\!\!\leqslant\! 0.5\%.$ 

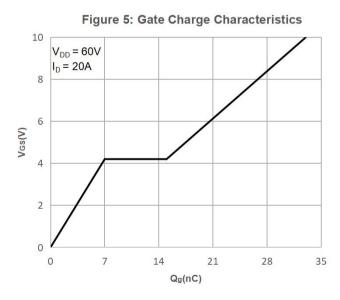
# **Typical Performance Characteristics**

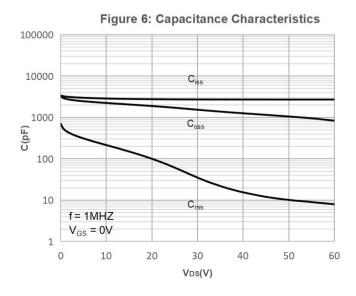
Figure 1: Output Characteristics 50 V<sub>GS</sub> = 10V 40  $V_{GS} = 6V$ V<sub>GS</sub> = 5.5V 30  $V_{GS} = 5.3V$ 20 V<sub>GS</sub> = 5.1V 10 0 0 1 2 3 4 V<sub>Ds</sub>(V)











# **Typical Performance Characteristics**

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

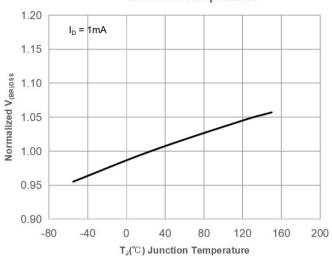
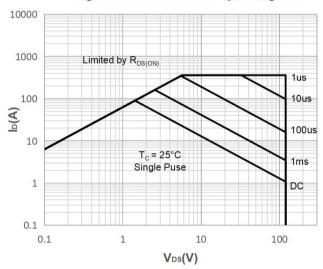


Figure 9: Maximum Safe Operating Area



**Figure 11: Normalized Maximum Transient** 

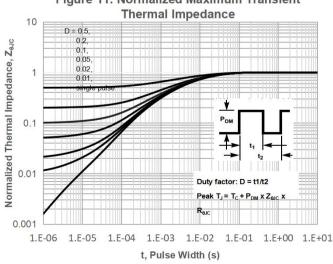


Figure 8: Normalized on Resistance vs.
Junction Temperature

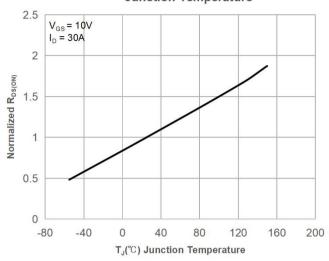


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

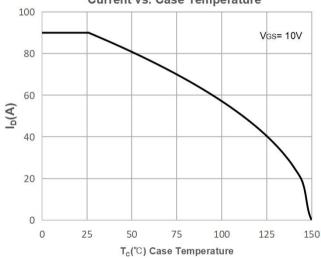
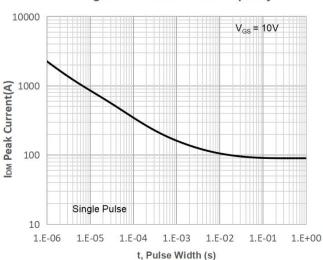


Figure 12: Peak Current Capacity



## **Test Circuit**

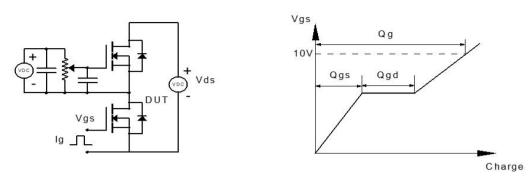


Figure 1: Gate Charge Test Circuit & Waveform

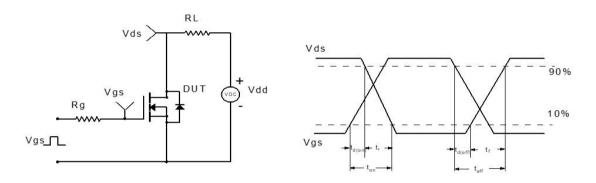


Figure 2: Resistive Switching Test Circuit & Waveform

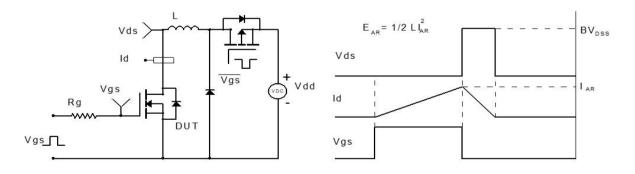


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

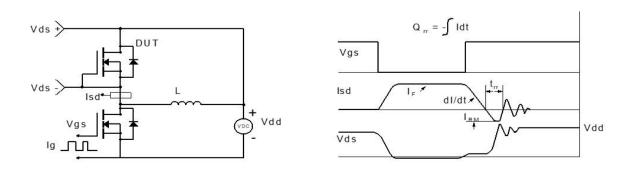
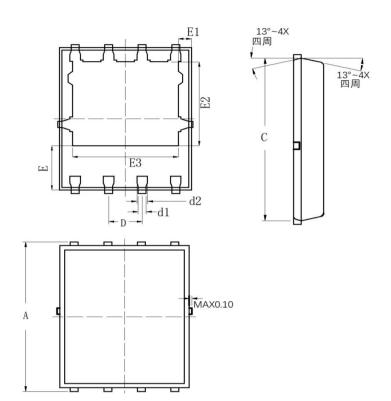
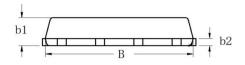


Figure 4: Diode Recovery Test Circuit & Waveform

## Package Mechanical Data(PDFN5x6-8L)





	COMMON DIM	MENSION (MM)			
PKG	PDFN 5×6-8L				
SYMBOL	MIN	TYP	MAX		
Α	6.000	6.100	6.200		
В	4.875	4.900	4.925		
b1	0.975	1.000	1.025		
b2	0.246	0.254	0.262		
С	5.775	5.800	5.825		
D	1.245	1.270	1.295		
d1	0.275	0.300	0.325		
d2	0.375	0.400	0.425		
Е	1.725	1.775	1.825		
E1	0.395	0.445	0.495		
E2	3.425	3.475	3.525		
E3	3.960	4.010	4.060		

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